CLAIMS:

1. A video signal processing circuit, comprising:

a GRAM which stores pixel data, which is data corresponding to pixels of a display screen, at least in the amount equivalent to said display screen, said pixel data being written in said GRAM in synchronization to a memory clock signal;

a latch circuit which reads and stores pixel data corresponding to pixels representing a scanning line of said display screen from said GRAM; and

a control means,

wherein said pixel data corresponding to said pixels representing said scanning line stored in said latch circuit is displayed on said display screen, and

in the case of contention between writing of said pixel data in said GRAM and reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM, said control means delays reading of said pixel data corresponding to said pixels representing said scanning line and controls so as to perform reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM once again.

2. The video signal processing circuit of claim 1,

wherein said control means comprises a delay means which delays and inputs a display read control signal and a data latch signal for said delay time during a period which is after a point at which said memory clock signal corresponding to writing of said pixel data in said GRAM is supplied, said writing accompanying said contention, but which is before supplying of the next memory clock signal following said memory clock signal so that said latch circuit reads pixel data corresponding to pixels representing said scanning line.

3. The video signal processing circuit of claim 2, wherein said delay time can be adjusted in a variable manner.

4. The video signal processing circuit of claim 1, wherein said control means comprises a monitoring means which monitors whether writing of said pixel data in said GRAM contends against reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM.

5. The video signal processing circuit of claim 4, wherein said control means comprises a delay means which delays reading of said pixel data corresponding to said pixels representing said scanning line based on a monitoring result obtained by said monitoring means and controls so as to perform

reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM once again.

6. The video signal processing circuit of claim 1, wherein when writing of said pixel data in said GRAM is executed plural times during a contention-free memory update period in which said pixel data corresponding to said pixels representing said scanning line are read to said latch circuit from said GRAM said control means upon occurrence of said contention delays reading of said pixel data corresponding to said pixels representing said scanning line between a period of writing said pixel data and a period of writing next pixel data, and controls so as to perform reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM again plural times during said contention-free memory update period.

7. A method of controlling a video signal processing circuit which comprises:

a GRAM which stores pixel data, which is data corresponding to pixels of a display screen, at least in the amount equivalent to said display screen, said pixel data being written in said GRAM in synchronization to a memory clock signal;

a latch circuit which reads and stores pixel data corresponding to pixels representing a scanning line of said display screen from said GRAM; and

a control means,

said method comprising a step at which in the case of contention between writing of said pixel data in said GRAM and reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM, said control means delays reading of said pixel data corresponding to said pixels representing said scanning line.

8. An integrated circuit in which the video signal processing circuit of claim 1 is incorporated.